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OEBSYS II LINE SCAN CAMERA INTERFACE SYSTEM

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INTRODUCTION

Visual inspection in industrial processes requires versatile, fast, and intelligent hard- and software. Rather than building a complete hardware system from the ground up, the OEBSYS II interface system makes use of a variety of standard computers, the Intel 80386 based on the PC/AT bus. 80386 computers are available with fast clock frequencies at reasonable cost; adding the OEBSYS II interface system creates a powerful yet inexpensive visual inspection system. OEBSYS II performs most image processing tasks in hardware for speed and ease of adaptation to a wide range of processes.

Drivers written in 'C' to talk to the system are provided with a set of hardware for system integrators and programmers.

THE OEBSYS II SYSTEM

The OEBSYS II camera interface system is a high performance camera controller and AT bus interface for Fairchild and EG&G Reticon line scan cameras. At the present time the system supports two 3456 pixel cameras (Fairchild 1600R) for an effective line length of 6912 pixels. EG&G Reticon LC1901 and LC1902 series cameras with 256 to 2048 pixels per line are also supported.

The system was designed especially for binary imaging and achieves its highest data rate for runlength encoded binary data generated on the board. 8-bit grey level data may also be transferred, although at a lower data rate because it is not encoded.

The system consists of a two board set (two 16-bit slots)with an external box for analog to digital conversion circuits and connectors for camera, synchronization pulses. It operates in a series of PC/AT 80386 systems. Maximum performance is achieved with 25 MHz or 33 MHz clock frequency computers. Depending on the cameras used, circa 4 Megabytes of RAM are required in the computer to store the data. Images can be viewed for setup and control on a VGA black/white or color monitor. The 80386 computer must have a diskette drive, hard disk, VGA output, and a serial or parallel port to talk to the outside world.

Since lighting uniformity is frequently a problem in binary applications, each camera pixel undergoes individual gain and offset compensation, the parameters for which may be computed and loaded at run time. In addition, special compensation circuitry corrects for bulb aging and the 120 cycle ripple inherent in AC tungsten light sources. The camera is currently run at clock rates up to 5 Mhz, depending on the camera used. In binary mode the effective camera speed is limited by the PC/AT bus speed and by the illumination available to the camera.

OEBSYS II CAMERA INTERFACE FEATURES

1. A double buffered run length encoder allows extremely high data transfer rates for binary acquisition. Camera data can be input to one buffer at the same time that the buffered data from the previous scan is being transferred to main memory. The transfer rate is further enhanced by 16 bit data transfers; two consecutive 8 bit run lengths are transferred at a time.

2. Single buffered 8 bit grey level data acquisition is provided in the event that grey level data is desired. Data transfers are 8-bit transfers, and in this case the camera data rate may exceed AT bus transfer speed. The digitized data is compensated by the offset and gain adjustment logic.

3. The run length encoder provides a typical 15 to 1 data compression as compared to pixel to bit mapping. Encoding is done in real time.

4. A digital signal processor allows individual dark offset and pixel gain compensation for each pixel. The compensation curves for a particular setup can be easily obtained and then saved to disk for future recall. This compensation can effectively minimize variations in: 1.) lighting across the image, 2.) pixel to pixel gain, 3.) pixel to pixel dark levels and, 4.) stray light in the camera chamber.

5. Exposure clocking can be internal or external (i.e., from a stepper table). The system switches automatically to external when input pulses are sensed. The internal exposure rate is programmable from 39 to over 1 million exposures per second. An exposure pulse rate divider is provided in case the actual camera exposure rate is a divisor of the external synchronization pulse rate. This is useful for synchronizing the camera to a translation stage. If desired, the exposure rate generator can be disabled and exposure pulses generated

manually through software.

6. The camera pixel data rate is tested to 7 MHz.

7. The interface can handle either one or two line scan cameras with up to 3456 pixels each.

8. Synchronization and vertical outputs for an oscilloscope are available for camera setup and monitoring. The switch or software selectable display can show either raw video data or the illumination compensated data. The binary threshold is multiplexed onto the camera display to facilitate lighting and threshold adjustment.

9. A TTL level input is provided so that the camera control software can poll the state of a microswitch. This may be used to determine the position of a mechanical positioning stage.

10. The run length encoder has two programmable digital thresholds that operate on the compensated grey levels to provide binary video. When set to different values, these thresholds implement hysteresis, providing exceptional noise rejection.

11. Buffer sizes are:

Run Length Data Buffers	Two 2K X 8
Grey Level Data Buffer	8K X 8
Offset Compensation Buffer	8K X 8
Gain Compensation Buffer	8K X 8

12. Two LEDs are provided; one indicates camera peaking (approaching saturation), the other indicates that the internal exposure generator is active.

13. A software activated test bar generator is included for testing both hardware and software. The generator has seven different test modes that test various aspects of the hardware.

14. An automatic gain control circuit is provided on the front end to compensate for variations in lighting due to AC line frequency and other factors. An external sensor is placed at or in the light source and two trim pots are adjusted using a procedure designed to facilitate the adjustment.

15. Boards operate at 8 or 10 Mhz ISA bus speeds.